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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 1, 2006  
Date

Alexandra Beggs  
Alexandra Beggs

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Brent Keeth  
Patent No. : US 6,819,611 B2  
Issue Date : November 16, 2004  
Title : METHOD AND APPARATUS FOR DATA COMPRESSION IN MEMORY DEVICES

Attorney Docket No.: 500426.02  
Serial No. : 09/964,113  
Filed : September 25, 2001

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Certificate**  
**AUG 10 2006**  
**of Correction**

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), References Cited, Other Publications	"Descriptive literature entitled, 400MHz SDRAM, 4Mx16 SDRAM Pipelined, Eight Bank, 2.5 V Operation, SDRAM Consortium Advance Sheet, published throughout the United States, pp. 1-22."	Descriptive literature entitled, "400MHz SDRAM, 4Mx16 SDRAM Pipelined, Eight Bank, 2.5 V Operation," SDRAM Consortium Advance Sheet, published throughout the United States, pp. 1-22."
Item (57), Line 1	"pair of arrays"	--pair of arrays,--
Column 4, Line 23	"November. 1991 and"	--November 1991 and--

**AUG 14 2006**

Column 7, Line 62	"appended claims. which"	--appended claims, which--
Column 8, Line 28	"gate of a transistor"	--gate of a transistor;--
Column 9, Line 5	"columns each column"	--columns, each column--
Column 9, Line 16	"complementary dais lines"	--complementary data lines--
Column 9, Line 57	"coupled a"	--coupled to a--
Column 10, Line 48	"and in"	--and an--
Column 11, Line 32	"transistor"	--transistor;--
Column 12, Line 41	"logic stare"	--logic state--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date:

July 31, 2006

By:

Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076

Dorsey & Whitney LLP

1420 Fifth Avenue, Suite 3400

Seattle, WA 98101

(206) 903-8785

Attorney for Applicant(s)

EWB:tdp

Enclosures:

Postcard

Form PTO-1050 (+ copy)

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PATENT NO. : US 6,819,611 B2  
 DATED : November 16, 2004  
 INVENTOR(S) : Brent Keeth

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

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MAILING ADDRESS OF SENDER:

**DORSEY & WHITNEY LLP**  
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